EE/CprE/SE 492 Status Report 2
Feb 6– Feb 12

Group number: **22**

Project title: **ReRAM Compute Asic Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - This week we continued working on our foundational modules. Layouts for 1T1R and TIA are nearly complete. Our harness has been decided (caravel) and can be brought into xschem and magic. Bringing other modules into the harness and precheck remain a problem, but hopefully this can be solved this coming week.
- **Past week accomplishments**
  - Vinicius Malaman Soares: Looked at past team's TIA design. Tested sddec23-13's comparator. Tried testing sddec24-13's 4bitADC testbench, had problems with some instances for some reason.
  - Tyler Kloser: Worked on the inverter to try to reach a stage to bring to precheck to understand how the process works
  - Ali Mannan: TIA layout is close to completion. No major issues were encountered, and a 2 stage op-amp design has been successfully brought into Magic for layout. Parasitics for TIA will be tested after successful layout.
  - Austin Miller: 1T1R layout was basically complete, but it didn't save correctly, so should be able to complete quickly again. Chipfoundry CLI project initialization working with xschem
- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: N/A
  - Austin Miller: reram simulations with CLI project not working as intended
  - Vinicius Malaman Soares: Fix some issues with 4bitADC instances.

- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Tyler Kloser	Precheck testing and understanding	5	11
Ali Mannan	Two stage op-amp to layout, connected as TIA	8	18
Austin Miller	CLI Tool updates, New project initialization script almost complete, 1T1R nearly complete (oops)	9	23
Vinicius Malaman Soares	Tested past team's comparator. Looked at TIA design for past team. Tried running the 4bitADC testbench (too many errors)	7	13

- **Comments and extended discussion**
    - N/A

Plans for the upcoming week

- Ali Mannan: Extract parasitics from TIA and work on bringing module through pre-check
- Tyler Kloser: Take inverter through precheck hopefully
- Austin Miller: Reram sims w/ CLI version of project, 1T1R through precheck
- Vinicius Malaman Soares: Fix the issue with some device instances on the 4bitADC testbench.

- **Summary of weekly advisor meeting**
    - Discussed current state of modules. Went through concerns of some devices such as resistors for TIA. Also discussed needs of testing by client and if we are the ones to set up tests entirely with code for the embedded RISC-V controller; we will be making most of the automated ones.